1as Jornadas de la Red RISC-V

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- **Título de la ponencia:**
  Overview of the RISC-V Core Market

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- **Abstract:**
  In this talk we'll cover the different offerings in the RISC-V Processor market and its recent evolution.

- **Biografía:**
  Roger Espasa got his Phd in Computer Science from Universitat Politècnica de Catalunya in 1997. Between 1999 and 2001 he worked for the Alpha Microprocessor Group on a vector extension to the Alpha architecture (see the Tarantula paper). In 2002, the Alpha team was acquired by Intel. between 2002 and 2014 Roger worked at Intel developing a vector extension for the x86 ISA which was initially deployed in the Larrabee and Knight's Corner product and then became the AVX-512 extension. Roger also led the team implementing the texture sampling unit for the original Larrabee chip. Roger also worked on the core for the Knight's Landing product (14nm) and led the core for the follow-on Knights Hill 10nm product. In 2014, Roger joined Broadcom where he worked on a from-scratch ARMV8 wide out-of-order core supporting both A64 and A32.In 2016 Roger founded SemiDynamics Technology Services where he is working on RISC-V cores. Roger has published over 40 peer-reviewed papers on Vector Architectures, Graphics/3D Architecture, Binary translation and optimization, Branch Prediction, and Media ISA Extensions. Roger holds 9 patents with 41 international filings.

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